AD-A041 754 WESTINGHOUSE ELECTRIC CORP HORSEHEADS N Y INDUSTRY AN--ETC F/G 20/12
MANUFACTURING METHODS AND ENGINEERING FOR TFT ADDRESSED DISPLAY--ETC(U)
DEC 76 D H DAVIES, W L ROGERS, T CSAKVARY DAAB07-76-C-0027
UNCLASSIFIED 77-8F9-PRODE-R1 NL

| OF |
AD
A041754

END

DATE
FILMED
8-77

SECOND QUARTERLY REPORT ON MANUFACTURING METHODS AND ENGINEERING FOR TFT ADDRESSED DISPLAY

for period of

August 7, 1976 to November 7, 1976

CONTRACT DAAB07-76-C-0027

placed by

PROCUREMENT AND PRODUCTION DIRECTORATE
UNITED STATES ARMY ELECTRONICS COMMAND
FORT MONMOUTH, NEW JERSEY 07703

with

WESTINGHOUSE INDUSTRIAL AND GOVERNMENT TUBE DIVISION
Westinghouse Circle
Horseheads, New York 14845

December, 1976

This project has been accomplished as part of the US Army's Manufacturing and Technology Evaluation for Thin Film Transistor Display Program, which has as its objective the timely establishment of manufacturing processes, techniques or equipment to insure the efficient production of current or future defense programs.

DISCLAIMER

The findings in this report are not to be construed as an official Department of the Army position unless so designated by other authorized documents.

DISPOSITION

Destroy this report when no longer needed. Do not return it to the originator.

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER

2. GOVT ACCESSION NO.

3. RECIPIENT'S CATALOG NUMBER

4. TITLE (and Subtitle)

(6) MANUFACTURING METHODS AND ENGINEERING FOR TFT ADDRESSED DISPLAY

5. TYPE OF REPORT & PERIOD COVERED
Second Quarterly Report
8/7/76 to 11/7/76

6. PERFORMING ORG. REPORT NUMBER
(14) 77-8F9-PRODE-R1

7. AUTHOR(s)

(10) D. H. Davies, W. L. Rogers, T. Csakvary, H. Y. Wey M. Green

8. CONTRACT OR GRANT NUMBER(s)
(15) DAAB07-76-C-0027

9. PERFORMING ORGANIZATION NAME AND ADDRESS
(1) Electron Dev (3)
Westinghouse Industry and Government Tube Div.
Westinghouse Circle
(2) Horseheads, NY 14845

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
2769781

11. CONTROLLING OFFICE NAME AND ADDRESS
Procurement and Production Directorate
US Army Electronics Command
Fort Monmouth, NJ 07703

12. REPORT DATE
(11) Dec [redacted] 76

13. NUMBER OF PAGES
43

14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)
As above
(12) 50 p.

15. SECURITY CLASS. (of this report)
None

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

~~Distribution limited to US Government Agencies only, contains Westinghouse Proprietary information.~~

DISTRIBUTION STATEMENT A
Approved for public release;
Distribution Unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

Approved for public release - distribution unlimited.

18. SUPPLEMENTARY NOTES

(9) Quarterly rept. no. 2, 7 Aug - 7 Nov 76,

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

transistors, thin films, electroluminescent, displays, vacuum, matrix, solid state

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This is the second quarterly report on Contract DAAB07-76-C-0027; Manufacturing Methods and Technology Evaluation for the fabrication of a thin film transistor based solid state display panel.

Progress in all scheduled tasks was made this quarter; the fabrication of the engineering samples (ES) through the use of a dedicated mask system is proving troublesome because of material interactions consequent upon the

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

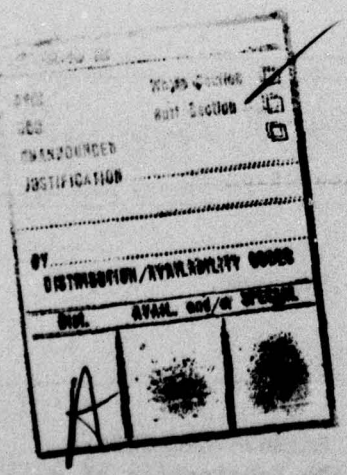
UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

rec 4/10 10:6

the use of the laboratory fabrication unit. Initial tests indicate that this specific problem will not be a factor in the pilot manufacturing machine. Displays were made in the ES format with an X-Y mask system. They had a similar thin film material layout to the pilot unit's requirements. The overall quality level was reasonably good and initial tests indicate the display should meet the required specifications.

The computer controlled pilot manufacturing unit is operating at overall satisfactory levels and good progress at reducing the level of elemental short circuits was made. All the tooling to make the displays on this unit is now ready and first complete displays from the pilot line are expected soon.



Document has statements A & B
Use statement A per Mrs. O'Brien,
Army Electronics Comd

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS AND FIGURES

ABSTRACT

This is the second quarterly report on contract DAA B07-76-C-0027; Manufacturing Methods and Technology Evaluation for the fabrication of a thin film transistor based solid state display panel.

Progress in all scheduled tasks was made this quarter; the fabrication of the engineering samples (ES) through the use of a dedicated mask system is proving troublesome because of material interactions consequent upon the use of the laboratory fabrication unit. Initial tests indicate that this specific problem will not be a factor in the pilot manufacturing machine. Displays were made in the ES format with an X·Y mask system. They had a similar thin film material layout to the pilot unit's requirements. The overall quality level was reasonably good and initial tests indicate the display should meet the required specifications.

The computer controlled pilot manufacturing unit is operating at overall satisfactory levels and good progress at reducing the level of elemental short circuits was made. All the tooling to make the displays on this unit is now ready and first complete displays from the pilot line are expected soon.

1. PURPOSE

The purpose of the present program is to establish the producibility of a Thin Film Transistor (TFT) Addressed Display by mass production techniques and with a mass production pilot facility. Existing quality control procedures will be improved, and where quality control systems are not in effect, they will be introduced. The major objective of the program is to originate production methods and techniques capable of meeting estimated military needs for TFT Addressed Displays for a period of two years after completion of the contract. A further objective is to prepare a base and an action plan which may be used to meet expanded requirements and, when necessary, to assist in establishing additional sources.

The significant tasks being performed during this reporting quarter include the following:

I. Establish manufacturing methods
IIa. Check the operation of the dedicated mask concept
IIb. Fabricate engineering sample displays
IIc. Test of engineering sample displays
III. Design, procure and debug equipment for circuit fabrication
IV. Design, procure and debug equipment for packaging process
V. Recipe development and cost reduction for circuit fabrication
VI. Recipe development and cost reduction for packaging process
VII. Design, procure and debug equipment for final test of displays.

A detailed description of the actual work performed and results achieved on each of these tasks will be given in the following narrative discussion. This report covers the period August 7, 1976 to November 6, 1976; if technically appropriate for continuity some discussion of the prior quarter results are included and so indicated.

2. GLOSSARY

Dedicated Masks - A set of metal aperature masks (usually 12) each with a segment of the overall thin film pattern. One mask is equivalent to one evaporation step.

X·Y Masks - A pair of contacting masks that are moved over each other to generate a complete set of thin film patterns. The one mask pair is used for all of the evaporation steps.

Packaging Process - This term is used to summarize all the steps that are needed to take the complete thin film transistor circuit through to a complete display. It includes laminar photoresist (RISTON(R)), phosphor spray and seal of the top plate.

RISTON(R) - This is a Dupont trade-name for their laminar (sheet) photoresist. We use the term to cover the process of applying the material through a laminator, exposing and developing the pattern of phosphor aperatures.

APPLICON(R) - This is a trade-name (Applicon Co.) that is used to summarize the computer aided design (CAD) system. This interactive design tool is used for pattern layout and to generate magnetic tape to control the MANN photorepeater.

MANN(R) Photorepeater - A commercial unit that generates exposed, patterned, photographic plates of ultra high

quality. These plates are used to generate the metal masks.

Anneal - A long, high temperature bake, given to the thin film circuits as part of their fabrication process.

3. RESULTS AND DISCUSSION

For clarity the narrative discussion of tasks performed and results achieved will be structured on the initial task outline as shown in the CLIN0002AA PERT Chart.

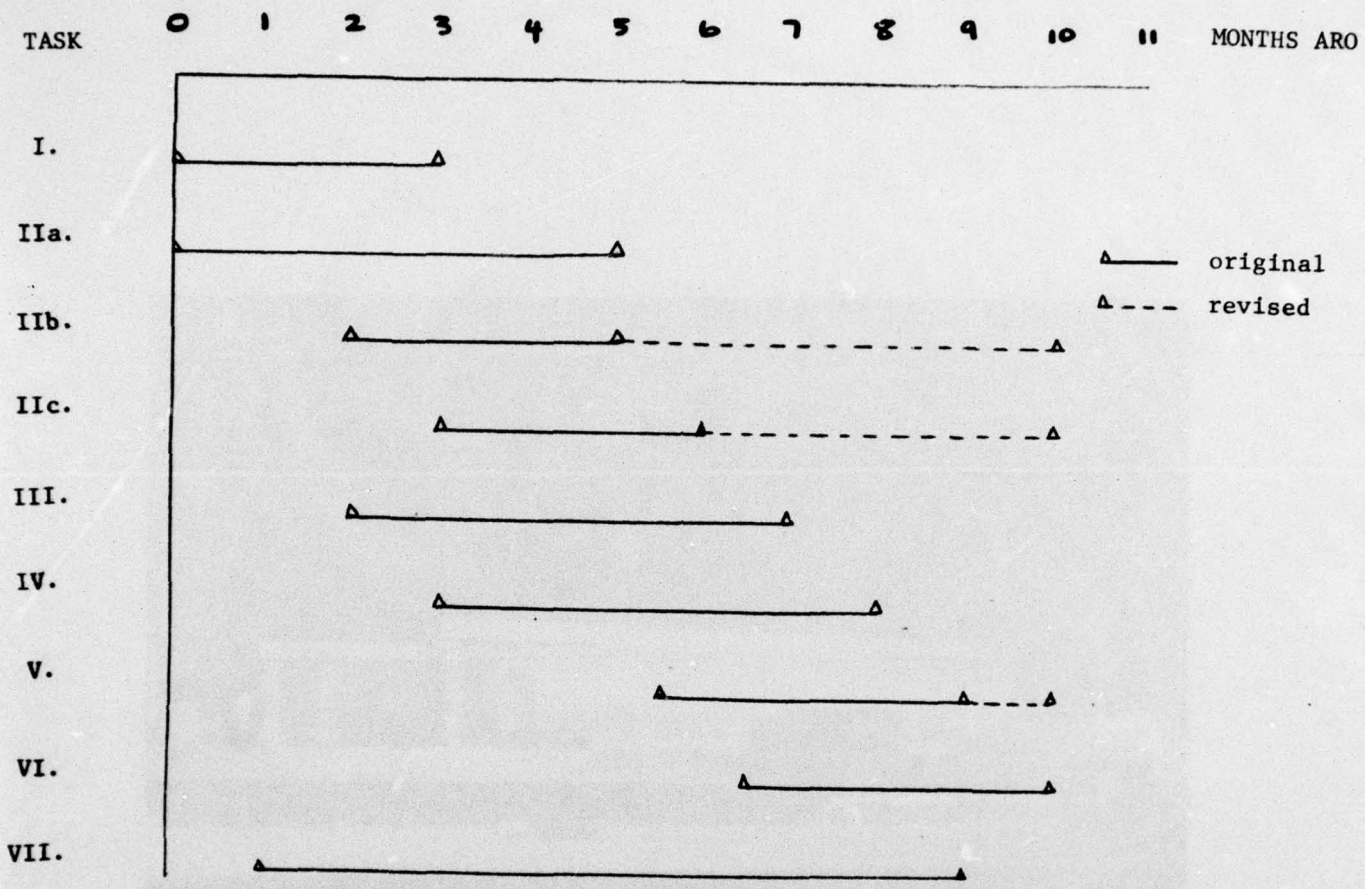
Fig (1) shows the task/time schedule for the first three quarters as revised and updated.

3.1. Task I. Establish Manufacturing Methods

This program phase includes effort using both the twelve station pilot manufacturing line and the laboratory six station unit. Specific tasks conducted include the following:

- Using the laboratory version of the pilot facility (the so-called "laboratory dedicated mask" machine), the operation of the magnetic pull-up fixture was checked in detail. The fixture is shown in Fig (2). No problems of significance to the pilot machine were found although specific malfunctions relevant to the engineering samples fabrication were observed, as described below. It was determined that the Teflon alignment pin bushings needed attention and/or replacement on a periodic basis. This information was conveyed to the pilot line personnel.

- The alignment of the mask set was checked using the split field alignment microscope. The procedure and equipment are used in common with the pilot operation. Pilot line personnel were then trained in the specifics of the display mask set alignment process. Some minor tooling modifications were needed to allow ready visual access to the alignment registration masks, otherwise this prealignment process has worked well.



I. Establish manufacturing methods

IIa. Check the operation of the dedicated mask concept

IIb. Fabricate engineering sample displays

IIc. Test of engineering sample displays

III. Design, procure and debug equipment for circuit fabrication

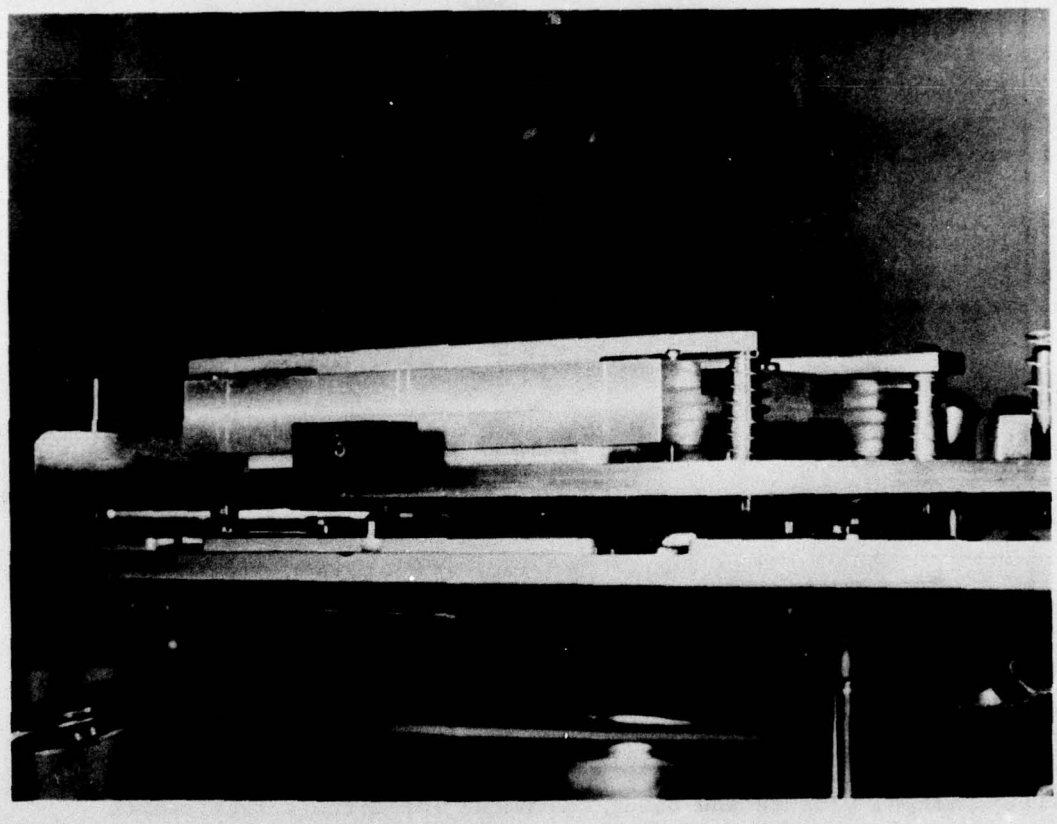
IV. Design, procure and debug equipment for packaging process

V. Recipe development and cost reduction for circuit fabrication

VI. Recipe development and cost reduction for packaging process

VII. Design, procure and debug equipment for final test of displays.

1. TASK/TIME SCHEDULE FOR FIRST THREE QUARTERS



2. MAGNETIC PULL-UP FIXTURE

• Initial deposition runs were performed with the basic 11 stage mask set, using the laboratory system. All the sequences checked out and the as-fabricated layout conformed to the original "Applicon" design layout. Fig (3) shows the cell layout as designed (from the "Applicon" CAD data base) and as actually fabricated.

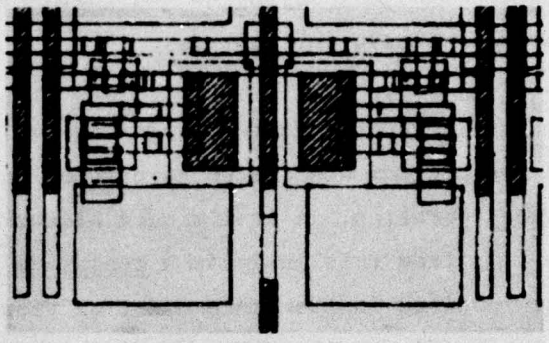
• A tentative unit cell electrical specification, derived from the research phase of the program was tested as part of the foregoing laboratory dedicated operation. A preliminary electrical specification is given in Table (1); from this analysis a tentative material recipe was generated that resulted in the achievement of these electrical specifications. Table (2) details that material recipe. Fig (4) shows actual measured device characteristics, taken from thin film transistors made on the laboratory unit, that meet these specifications.

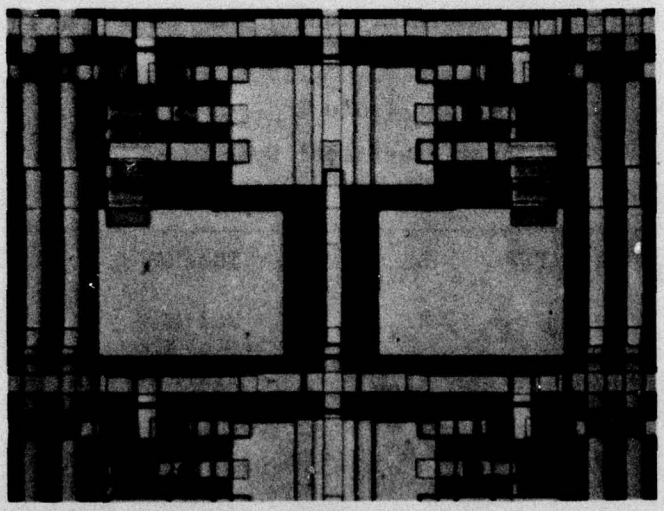
Table 1

Tentative Electrical Specification

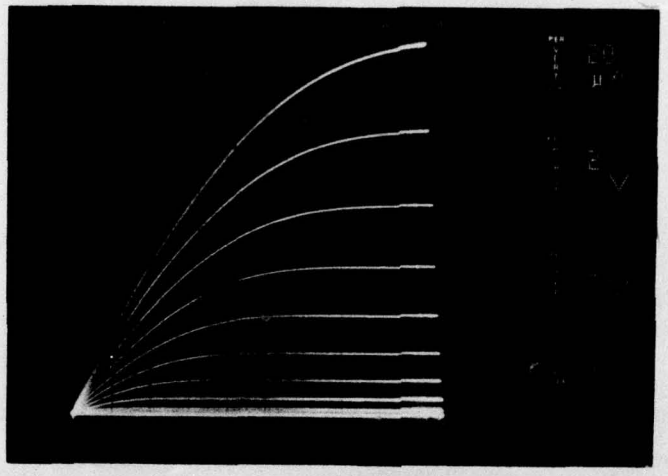
Device	Parameter	Requirement	Achieved
T_1 logic TFT	I_{ON}	> 100 μA	300 μA
	R_{ON}	< 0.1 MΩ	30 kΩ
	I_{OFF}	< 2.5 nA	1.0 nA
	V_B*	> $50V_{pp}$	>>$50V_{pp}$
T_2 power TFT	I_{ON}	> 125 μA	350 μA
	R_{ON}	< 0.8 MΩ	∿100 kΩ
	I_{OFF}	< 7 μA	1 μA
	V_B	> $200V_{pp}$	$300V_{pp}$

*Breakdown limit



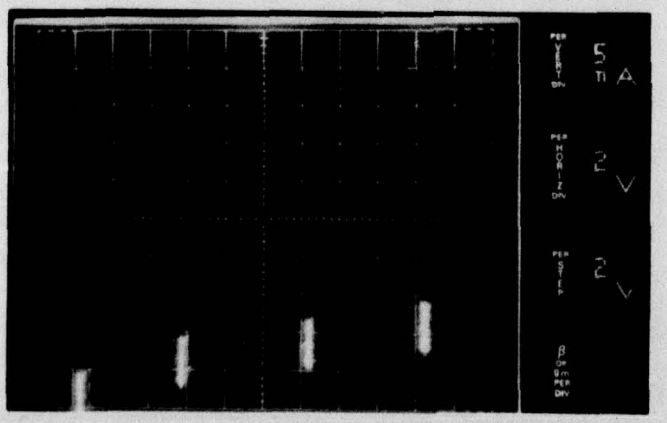


3. DESIGNED CELL LAYOUT AND AS ACTUALLY FABRICATED LAYOUT



Typical Display TFT

Power Device at High Voltages



Leakage in Logic TFT
V_{GS} = -10V

4. MEASURED TRANSISTOR CHARACTERISTICS TAKEN FROM TYPICAL DISPLAY CIRCUITS

Table 2

Initial Material Specification
to Achieve Electrical Requirements*

TFT gate dielectric	Al_2O_3	5000Å/each gate
Capacitor dielectric	Al_2O_3	5000Å/two layers
Crossover dielectric	Al_2O_3	> 1.5 μm
Bus bar metal	Al	1000Å
Transistor gate metal	Al	1000Å
Transistor semicondutor	CdSe	100Å
Transistor source/drain metal	Various; e.g. Au	1000Å

*Derived from initial manufacturing methods, Task I.

3.2. Task I. Establish Manufacturing Methods - The Pilot Machine

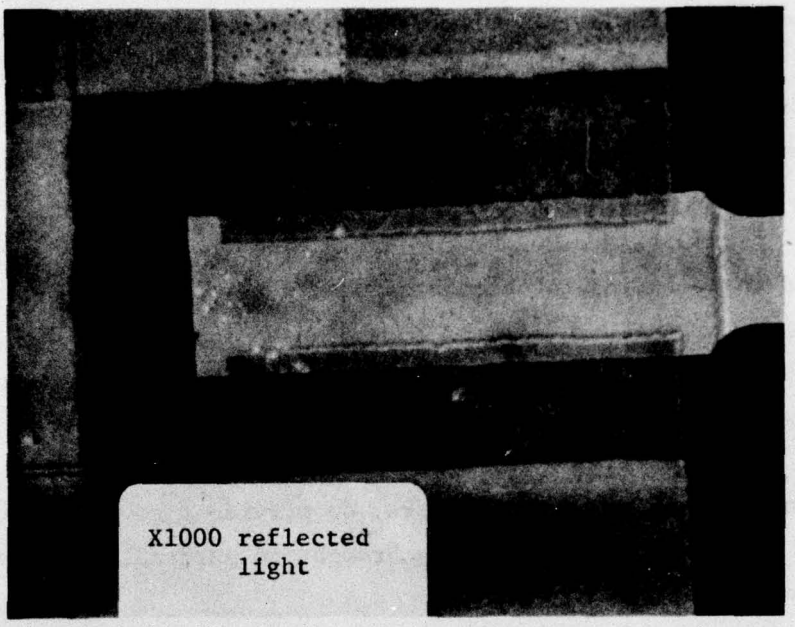
The first tasks on the pilot machine were to check the basic operation of the process/material system regarding certain basic requirements, such as shorting, under conditions that utilize the new magnetic pull-up fixturing without the added constraint of the new masks and new substrate holder tooling. From this initial analysis it was hoped that critical problem areas could be pin-pointed early in the program.

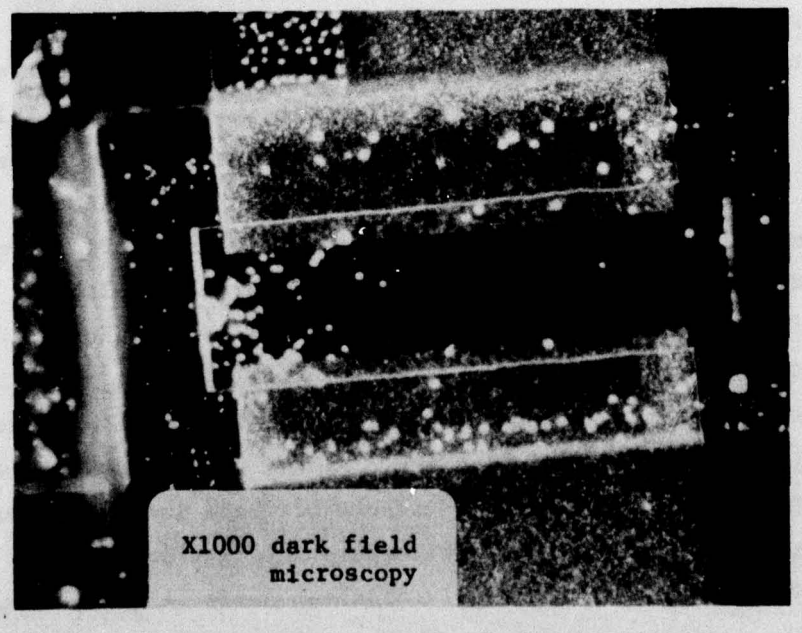
To quickly move into this program phase a simple test circuit was used. It has 4000 test transistors of similar dimensions to those required in the display. The masks are also ~4" square and, although less "dense" than the eventual masks, do provide a good initial test vehicle. The test transistors are brought to external pads for easy testing of shorts.

Using the tentative material specification the problem of shorting in the circuits was examined. As determined in the engineering samples program, this will be a key problem. A detailed discussion of various causes for circuit shorts was given in the first quarterly report. In that report considerable success was reported. This present analysis indicates that two probable major causes of internal short circuits in thin film, large scale integrated circuits remain: inclusions in the insulator material and interactions between materials (specifically indium or cadmium selenide with the other materials).

The "inclusions" referred to here are quasi-spherical particles, ranging up to two or three microns in size, which occur primarily in the transistor gate area, but also in areas with insulator films only. Fig (5) illustrates these inclusions. A very strong statistical correlation exists between the incidence of these inclusions and the incidence of short circuits. Preliminary information tends to suggest that these inclusions are actually aluminum oxide (Al_2O_3), which is used as the insulator material. This preliminary "information" is derived from the following:

1. Inclusions with this geometry can be found in areas of the substrate that are masked off from every evaporant source except aluminum oxide.





5. INCLUSIONS IN INSULATOR AREAS

2. Initial analyses by secondary electron emission analysis from a scanning electron microscope always indicate the presence of insulator material only, in areas with inclusions where only insulator material is known to be present.

Additional investigation is planned for the very near future using other sophisticated analysis instrumentation available at the Research Laboratories.

On the assumption that these inclusions are aluminum oxide, experimental processing was performed on test circuits (awaiting display panel tooling), using different techniques and different procedures to evaporate aluminum oxide, to eliminate these inclusions. High-rate, radio-frequency sputtering has been attempted, but initial indications are that this technique has a new set of problems which will require significant effort to overcome. Current efforts are now pointed toward modifying procedures for electron beam evaporation. Three different source materials have been used, with varying degrees of success. Single crystal sapphire appears to cause "sputtering." Vacuum-sintered alumina (Lucalox) has fewer inclusions but they are still statistically significant. The same holds true, perhaps to a slightly lesser extent, for a vacuum-melted alumina from the Merck Company, designed specifically for electron-beam evaporation. Procedural changes involving beam focussing, sweep focussing, and different evaporation rates are also being investigated.

At the same time, experiments to determine the effect of indium (adhesion layer) concentration are being carried out, as indium is by far the most active material present and melts well below any reasonable annealing temperature. It is, therefore, the most likely suspect in any material interaction. Within the process development facility, these experiments will be limited to changing the concentration of indium, as scientists in the research area are investigating other materials to replace indium as the adhesion layer for conductors.

3.3. Task II. Fabrication of Engineering Samples and Operation of Dedicated Mask Concept

The fabrication of the engineering samples is slightly behind the pre-established schedule submitted to the Army in the program PERT chart. Note however that significant progress has been made and several months remain relative to the formal ES delivery date. It is perhaps relevant, nevertheless, if we examine in some detail the problems (and solutions) that have been determined so far in this program phase.

(a) Poor pattern definition

This is a consequence of the lack of mask/substrate contact, despite the best magnetic pull-up technology we know how to incorporate. We have in previous months pinned down this problem to excessive thermal effects in the ES device fabrication unit. Two parrallel solutions were implemented to solve this system deficiency; an extension of the evaporated throw distance and the incorporation of, IR reflective, heat shield, pull-up backing plates.* It can now be stated with confidence that these modifications have solved the problem at least as far as the ES samples fabrication unit is concerned and, since implementation, no fuzzy patterns have been observed.

(b) High resistance contacts on bus lines

Due to the 6 station ES system limitation we have to break the process half-way through the cycle. This process "break", which is only directly applicable to the ES fabrication but could have implications regarding the pilot machine, results in oxide film build up on aluminum surfaces. The high resistances formed cause excessive voltage drop on the gate busbars. A "flash" of evaporated gold, deposited through a mask in the sequence, eliminates the oxide film. Tests of contact resistance from inside the cells to edge contacts are summarized in Table (3).

*These backup plates are 5 mils Kovar sheet with etched apertures corresponding to the required mask openings. They are pretreated with copper to make them IR reflective.

Table (3)

Typical Contact Resistances

(1)	Direct source bus (Al) to source contact (Cr:Au)	= 30 Ω
(2)	Source bus to source contact via 2 complete extra cells	= 60 Ω
(3)	∴ Internal source bus contact/cell	= 15 Ω
(4)	Direct gate bus (Al) to gate contact (Cr:Au)	= 40 Ω
(5)	Gate bus to gate contact via one extra cell	= 80 Ω
(6)	Intra cell ground to ground bus	= 13 Ω
(7)	Intra cell ground to ground bus and one extra cell	= 20 Ω

(c) Equipment malfunction (laboratory ES samples unit)

We have not been severely constrained by equipment down time but it has been a contributory factor. Problems met with and resolved include poor bushing repeatability, excessive vibration in the system, poor reliability in the magnetic pull-up actuator feed through and miscellaneous leaks. The actuator problem is still a potential source of difficulty although it operates satisfactorily now.

Despite the satisfactory resolution of the above problems we still do not have quality displays. To determine why we set about establishing a detailed test procedure. Mr. Paul Malmberg has been made the key test engineer on the ES samples so that we can get focussed effort on this aspect. The test for insulator is as follows.

Dielectric, intrinsic quality test

Using ES Samples #D48 an experiment was carried out to determine the quality of gate insulator and to correlate insulator breakdown (if possible) with particles or spots under the gate metal as viewed through a 400X microscope. A sampling of 60 power transistors was made, taking 15 devices from each of the four corners. The electrical test

consisted of tying the source and drain together at ground, applying a positive sweep voltage to the gate and recording the voltage at which the first breakdown event occurred.

Results of the test show overall adequate insulator quality and no direct correlation between defects and voltage breakdown although visual inspection after the test showed approximately 4 breakdowns which occurred at an observed defect site. Breakdown appeared to be a function of position on the substrate and probably more closely related to alignment and metal deposition. For example, in one corner where the gates were obviously misaligned breakdown occurred along the non-overlapping edge. In another corner, breakdown was primarily at the side of the gate but at either end of the semiconductor (most often at the open end of the gate). In summary, breakdown appeared to be deposition sensitive, but independent of the miscellaneous spatter. Average breakdown voltage/spots were as follows 159/13, 164/38, 210/3, 244/17.

Conclusion: No obvious dielectric intrinsic quality problem.

The outlined results of the test program are shown in Table 4.

The overall conclusions were clear.

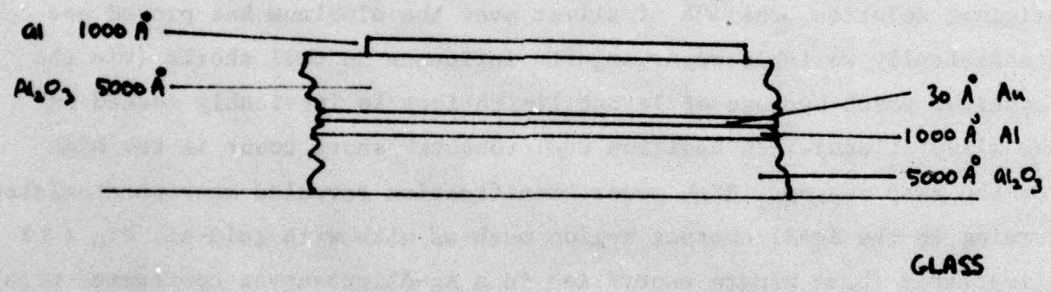
(a) The TFTs are close to specification and are not the limitation, see Fig (4) above.

(b) The intrinsic electrical properties of the Al_2O_3 dielectric are adequate and are not the limitation.

(c) There are excessive gate to ground shorts.

This latter item is obviously the key and so we attempted to track down the reason causing the shorts.

A series of runs were made with simple crossover circuits, i.e. only using a portion of the mask set. Every gate to ground and source to ground contact was checked and the individual shorts traced. It was immediately clear that a large number of the crossovers were shorted despite the high intrinsic breakdown in the Al_2O_3. These crossovers include a structure, as shown in Fig (6), that is a mixed

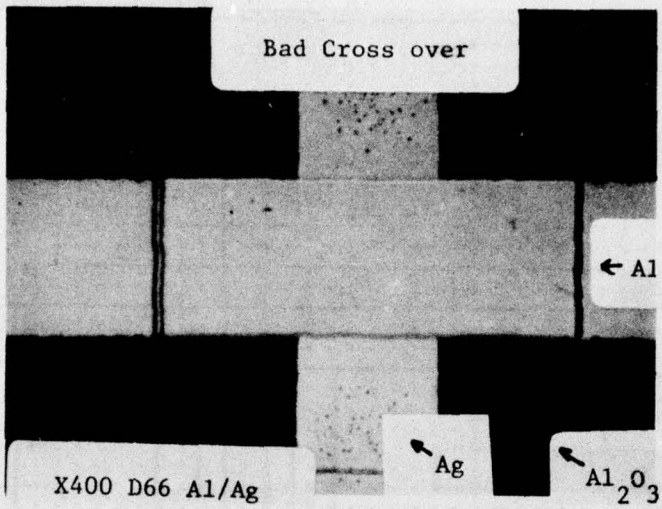


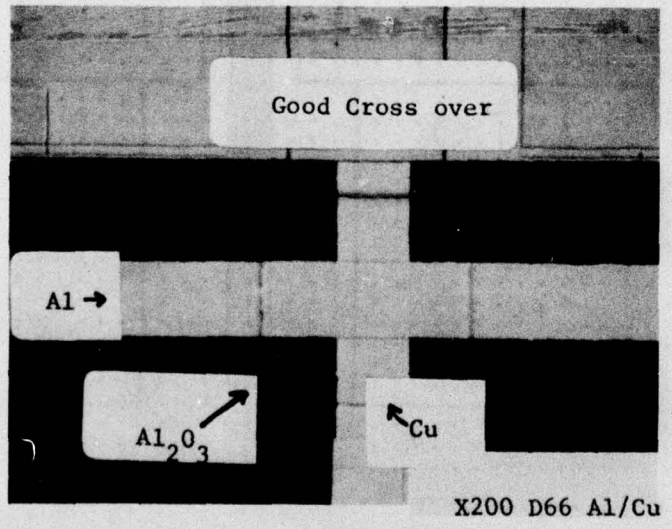
6. CROSS-OVER MATERIAL SYSTEM THAT GIVES RISE TO SHORTING

metal [Al-Au-Al-Al_2O_3-Al] system. The Au being a consequence of the flash (oxidation prevention) process detailed above. Small traces of black specs could be seen at the metal edge; it is now obvious that at the fringes of the mixed metal system an intermetallic Al-Au compound is forming and that this is causing the shorts.

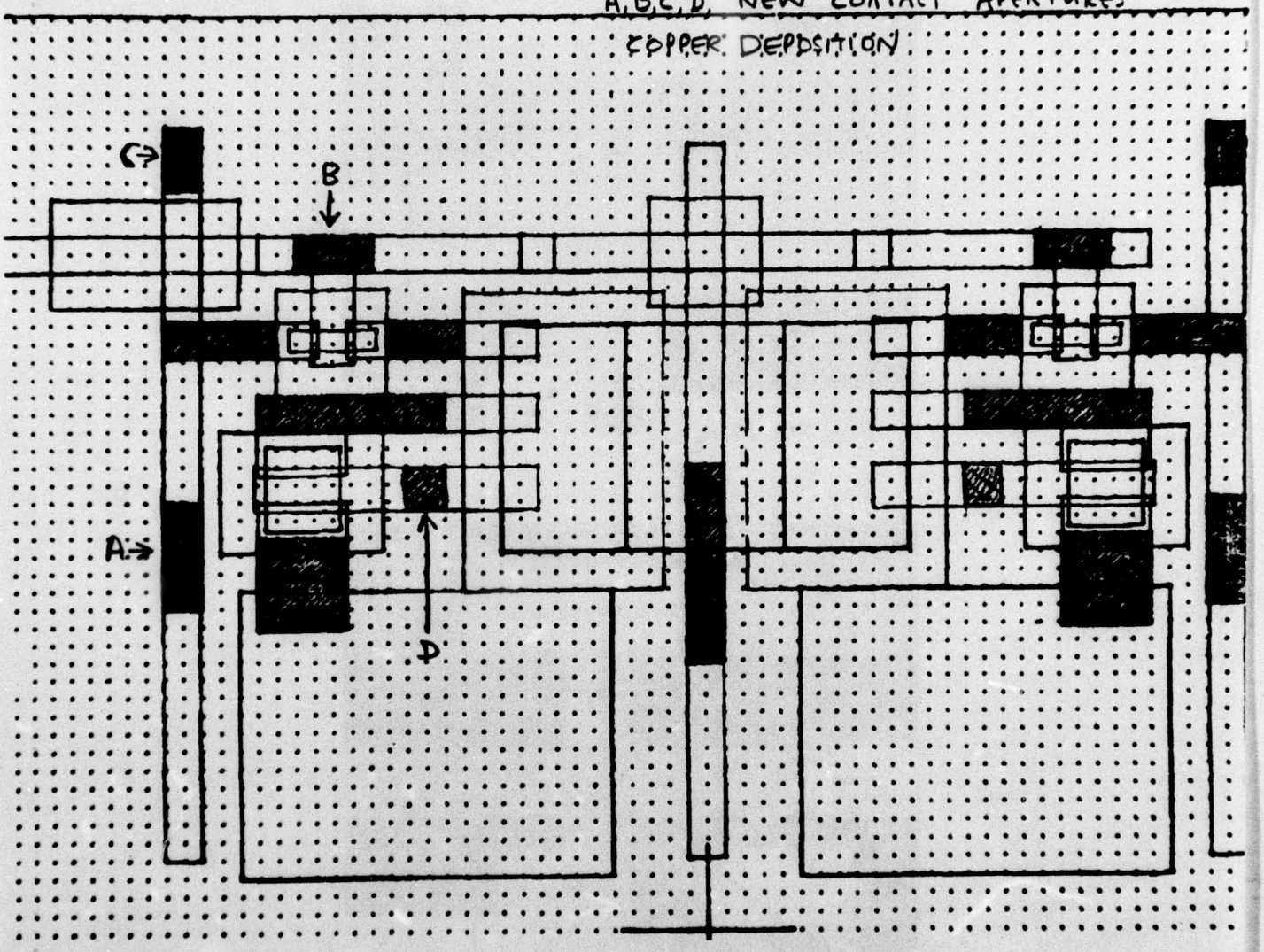
To check this idea a "pure" Al-Al_2O_3-Al crossover (No Au) matrix was made under identical conditions to the previous runs. It was free of the black intermetallic specs and largely non-shorted. The few residual shorts were explainable as the normal consequence of the Al_2O_3 deposition as discussed in detail below.

The use of silver as a protection flash coating over the aluminum has been tried. This is the aluminum that is exposed through the opening of the vacuum system half-way through the process. One original solution, the 40Å of silver over the aluminum has proved not statistically reliable regarding its influence on cell shorts (via the capacitor which because of layout limitations is inevitably coated in the silver flash). In addition the crossover short count is too high for the same reason. High power magnification revealed microparticulates forming in the Ag-Al contact region much as with with gold-Al. Fig (7) illustrates these minute asperities in a Ag-Al crossover contrasted with a good Al-Al crossover. Any asperity in a crossover can cause shorting. A better answer is needed and the obvious answer is to design a mask that applies this "flash" oxidation protection only over the selected areas that require protection not over the metal in the crossover region. Using our "Applicon" design data base we have examined this problem and decided that by minor modifications to MASK #7 (Copper interconnect) we can quickly obtain such a solution. This new mask has been layed out and is now ready for photofabrication. It should be received in 2-3 weeks. Fig (8) illustrates the modification to MASK #7.





7. MICROPARTICLES IN GOOD AND BAD CROSS-OVERS



8. MODIFIED MASK #7 LAYOUT

Table 4-A

Dielectric Test Date

0	0	3	1	5	4
200	240	215	250	245	230
0	0	0	0	0	3
235	225	205	240	270	240
0	1	0	0	0	0
230	195	230	205	245	260
1	0	1	0	1	0
150	245	175	215	240	275
0	0	0	0	0	3
180	200	220	245	255	250
210 $\overline{V_B}$		3 spots	244 $\overline{V_B}$		17 spots

Number of specs
$V_{G/SD}$ to break down

0	6	0	13	0	13
200	140	140	195	105	200
1	0	4	0	10	5
170	200	160	145	192	195
0	2	0	3	13	4
120	180	90	168	68	173
0	0	1	1	4	6
95	200	172	175	135	132
1	0	2	4	3	1
190	145	170	200	180	200
159 $\overline{V_B}$		13 spots	164 $\overline{V_B}$		88 spots

Table 4-B

Shorting Analysis

Sample No.	Gate to Ground	Source to Ground
D54	18	4
D53	16	10
D47	18	2
D48	29	3
TOTAL POSSIBLE	56	80

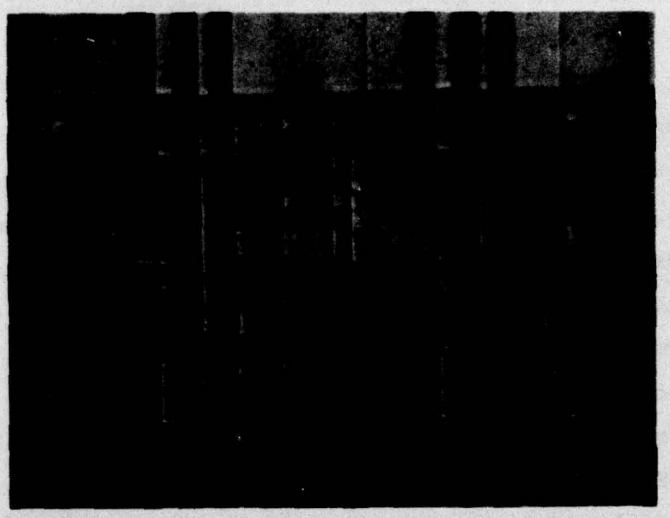
1 kΩ scale VOM test.

Conclusion: Defective gate to ground

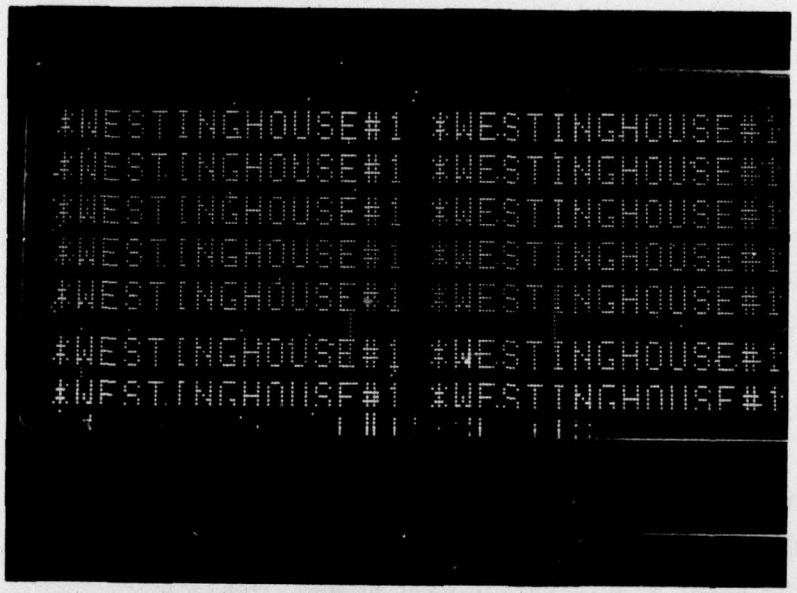
Although this problem is specific to the engineering samples program it is very valid to future pilot run activity. The opening of the vacuum system that causes the oxidation does not of course appertain in the pilot operation. In future rapid production rate runs however it is possible, indeed likely, that oxygen bleed-in may be needed to preserve Al_2O_3 stoichiometry. Such an oxygen depletion in the dielectric can occur with fast e-beam deposition rates such as would be needed with rapid production rates.

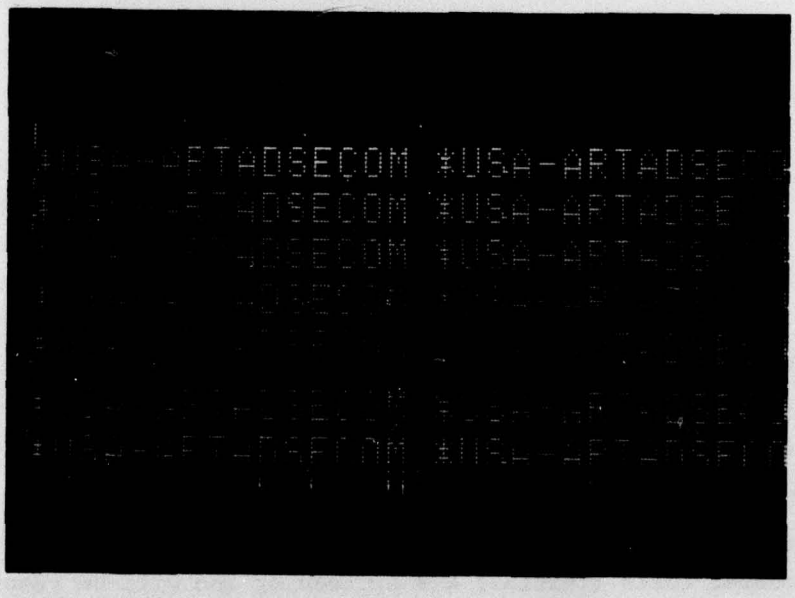
After receipt of the mask we will immediately incorporate it in ES fabrication. Meanwhile we are proceeding to attempt an alternate solution, viz; other material systems that could be less reactive as regards the generation of shorts.

To examine the validity of the thin film layout we decided to fabricate displays, in the required engineering samples format, using the X-Y movable mask approach. This method, that was the technique used to develop the technology originally, can reproduce the cell layout and material system used without difficulty, although it should be noted it is not a method directly applicable to the pilot operation. The mask purchase, jig modification, process establishment and actual deposition of these X-Y TF circuits is covered by an existing Army R&D contract (DAAB07-72-C-0061) and is therefore not charged to this MM&TE effort. The analytical comparison conducted between the circuits made with X-Y and the dedicated methods is however valid and of great interest. Fig (9) shows the layout used in the X-Y approach and Fig (10) shows the display so fabricated. As can be seen even with this limited effort we were able to rapidly achieve fabrication of reasonably good quality displays. This confirms us in the belief that there are no layout or material problems. Comparison of the TFTs themselves indicates that there are also no differences. The major ambiguities between these successful X-Y fabricated displays and the comparatively unsuccessful dedicated displays are:



9. CELL LAYOUT USED IN X·Y DISPLAY FABRICATION





10. DISPLAY OPERATION (X·Y FABRICATION METHOD)

(1) X-Y devices are fully populated rather than 5x7 blocks

(2) No shared common ground bus in the X-Y

(3) Use of the silver "flash" in the dedicated mask method.

The first two factors should not have any effect of significance; to check we will proceed immediately to make fully populated dedicated displays. The only major difference is the silver "flash", we remain convinced therefore that this is the root of our problems; next quarter should see this resolved via the new mask described above.

3.4. Task II. Test of Engineering Samples

Using the two good quality displays made to date we have conducted some quick estimations of how the displays measure up to the required final device specification. It is clear that, at least to date, the power specification will be met, Table 5.

TABLE (5)

POWER DISSIPATION

Spot brightness fl	No. of characters 0	64	128	256
20	250	240	290	390
30	240	-	-	550

Weights were within the 5 oz. limit and brightness levels were satisfactory and within the limit Fig (2.6) of the first quarterly report . Some defects (shorts and open lines) were present so that some difficulty in meeting the legibility/recognition specification was expected.

Improved quality can be anticipated as the program progresses. Environmental tests (initial) are proceeding and will be reported on in the next quarter.

3.5 Design, Procure and Debug Equipment for Circuit Fabrication

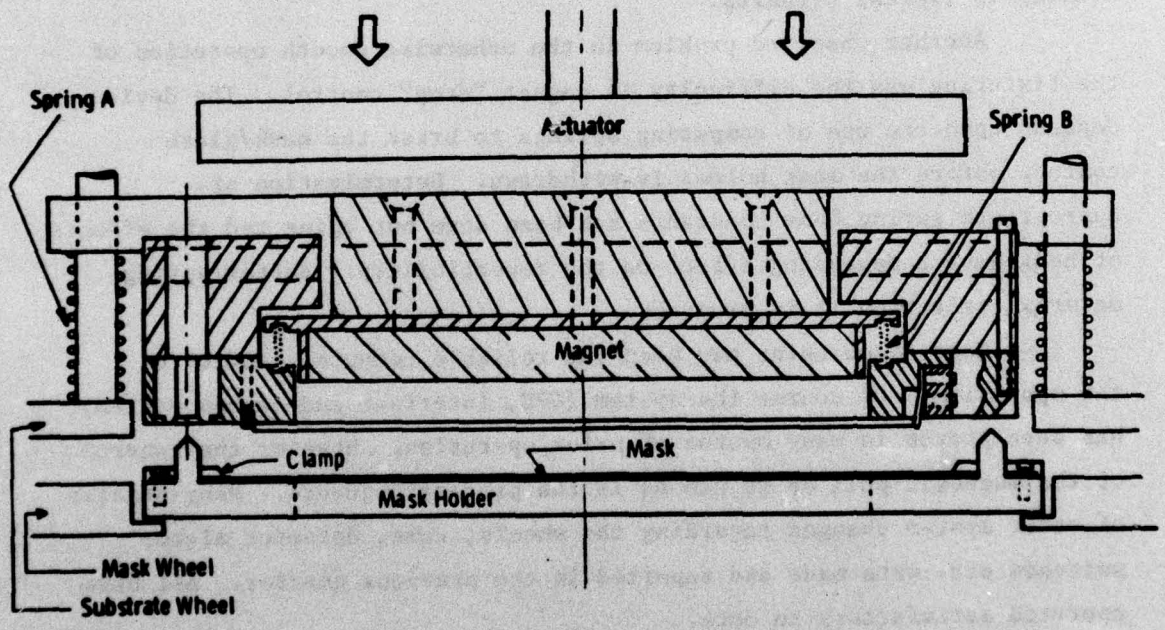
3.5.1.Task III-A. Design, Procure and Debug Equipment -- Internal Tooling and Fixturing for Circuit Fabrication

During this problem solving phase the operation of the magnetic pull-up fixturing the new substrate holders and the new mask holders has been observed. A cross section of the fixture is shown in Fig (11) and a picture in Fig (2). The first test is the ability of the jig to reproduce the present alignments, i.e., transistor gate overlaps, insulator pad locations relative to crossovers, location of the semiconductor, etc. In general this has been good throughout this period. However some irreproducibility due to pin/bushing/hole wear was observed. This will require some attention. Fig (3) shows the good registration overlap in typical circuits.

Another observed problem in the otherwise smooth operation of the fixturing was the difficulty in magnet "drop" control. The device depends upon the use of competing springs to break the mask/glass contact before the mask holder is withdrawn. Determination of appropriate spring force constants has been done but aging and the effects of heat have a degrading effect on the repeatibility. Better spring material selection is in progress.

Most encouraging has been the reliable computer control of the operation. Of course the system (CPU, interface and vacuum system) has been proven in many months of prior operation. However the control of the magnetic pull up is new as is the process sequence. Many details of other system changes regarding the wheels, cams, detector microswitches etc. were made and reported in the previous quarter. All have operated satisfactory to date.

The overall operation of the modified system and pull-up fixture, in conjunction with the associated substrate and mask holders, was deemed satisfactory. Some minor changes were made to the designs to reduce weight and to improve the pin-hole alignment through "coning" the hole aperture. A go-ahead was given to the tooling fabricators and four sets of magnetic pull up fixtures, substrate holders and 11 mask holders ordered to our specifications. They have recently arrived and their initial operation is described in the Section V report below.



11. CROSS-SECTION OF MAGNETIC PULL-UP FIXTURE

3.5.2. Task III-B. Design, Procure and Debug Equipment-Aperture Masks and Mask Pull-ups

The Ni-Cu:Be-Ni aperture masks developed for this program represent among the most advanced species of the mask makers art. Fig (12)shows a typical mask at high and low magnification. All the layouts, computer aided design, tape output conversion (to a compatible form with the Mann 1600 unit), and Mann photoplate generation was completed prior to the start of the program. A complete mask set had been purchased and during this reporting quarter effort at the pilot operation and as part of the engineering samples fabrication has been expended to prove out this aspect of the process. The major questions to be resolved in this debug phase were as follows:

(a) Are the masks too fragile to be effectively handled?

(b) Are the masks too fragile to be repeatedly cleaned?

(c) Is the magnetic permittivity sufficient to allow good pull-up, i.e. intimate glass/mask contact.

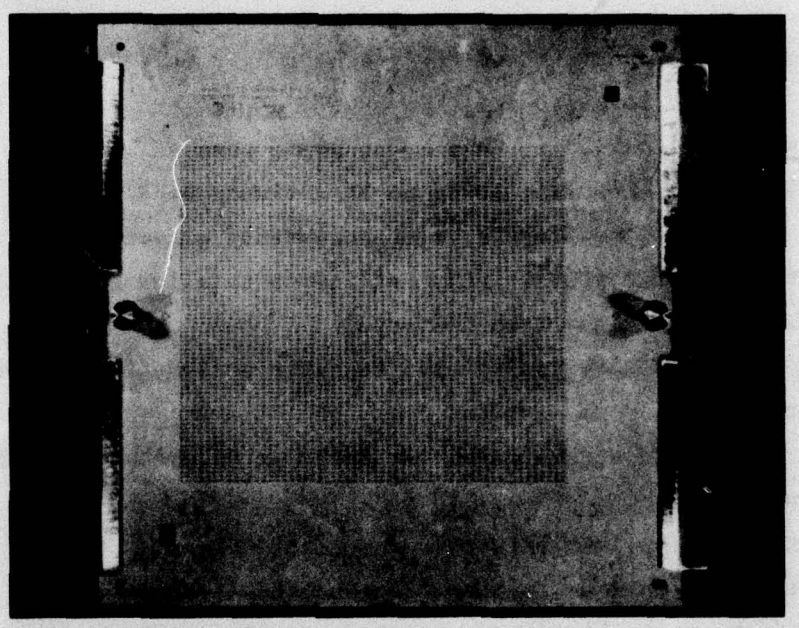
(d) Can the masks survive repeated magnetic pull action without distortion.

(e) How much deposited material can build up before peel of the films occur.

(f) What is the optimum thickness and metal core/skin ratio

(g) What is the optimum "natural" Be:Cu bend direction.

Several of these questions have now been resolved and the questions remaining are those of degree that can only be adequately determined in Task V. It is now clear that the masks can be handled and used. They can be cleaned but are also indicating slight evidence of delamination A better cleaning procedure, avoiding for example destructive ultrasonics, will be investigated in Task V. Heat has proved a major difficulty with these fragile masks; this problem is treated in more detail in the discussion of Task II (Engineering Samples) and Task V. Ripple distortions occur under the combined action of the multiple surface magnetic poles and heat. The use of thicker masks (∿5.5 mils) was indicated by this result but the resulting stiffness tends to induce "oil-canning", i.e. a popping of the Mask. No further mask changes are



12. TYPICAL APERTURE MASK

readily available within the short time frame but the use of secondary pull-ups has been a significant factor in alievating this problem. See Task II. Tests of alternate bow directions were made, i.e. the direction relative to the mask defining side that the pull-up (secondary) mask core is pulled from its coil. It is now evident that concave-up, towards the magnet, is the better direction for mask:glass intimate contact.

Orders for complete mask sets using the optimum parameters were placed with the supplier (Towne Labs Inc). Since receipt a single (from 222x77 = 17094) blocked aperture in the semiconductor mask was detected. It has been traced to the master photoplate and a corrected plate made. The aperture problem is trivial as of now. In addition a design error in one of the pull-up masks was found; an entire row of insulator apertures was partially blocked. The result was a partial short along an entire row. Once again quick access to the design tools meant that we were able to generate a new pull-up mask and it has already been received.

3.5.3. Task III-C. Design, Procure, and Debug Equipment - In Process Test Equipment for Circuit Fabrication

The question of test equipment to determine the critical "process-or-not" decision will be of vital importance to the success of the program as the circuit throughput increases. Not only does every circuit (half display) have 111x77 cells each with two transistors and a capacitor, but there are also 17,094 busbar crossovers per half display. Of course it is not necessary to test every device as statistical tests are sufficient. However a complete test would provide us with a method of pin pointing exact short (or open) sites, thus inidvidual causes can be identified, i.e. what caused the short. Also the possibility of elemental "repair" functions are raised.

A conceptual design for an automatic prober was put together. This system design was based largely on existing computer based automatic wafer probers. Fig (13) illustrates by block diagram the overall design. This equipment will be purchased on Westinghouse funds and will be used on the contract. Several suppliers were contacted and various vendors qualified. Test substrates with various metallizations (aluminum, copper and gold) were taken to the Semicon East Show (Long Island, NY) for probing. Visual inspection of probe marks made by an Electroglas Model 1034X automatic waferprobe with beryllium copper probe tips indicate that good electrical contact can be made on all of these materials (even breaking through the oxide layer on top of aluminum) without excessive damage to the conductors. Formal quotes from waferprobe vendors were received. An order for the complete system was placed. Shipment is expected in the second quarter of 1977. A further period will be needed to interface to the H-P minicomputer that will control the probe and record and analyze the data.

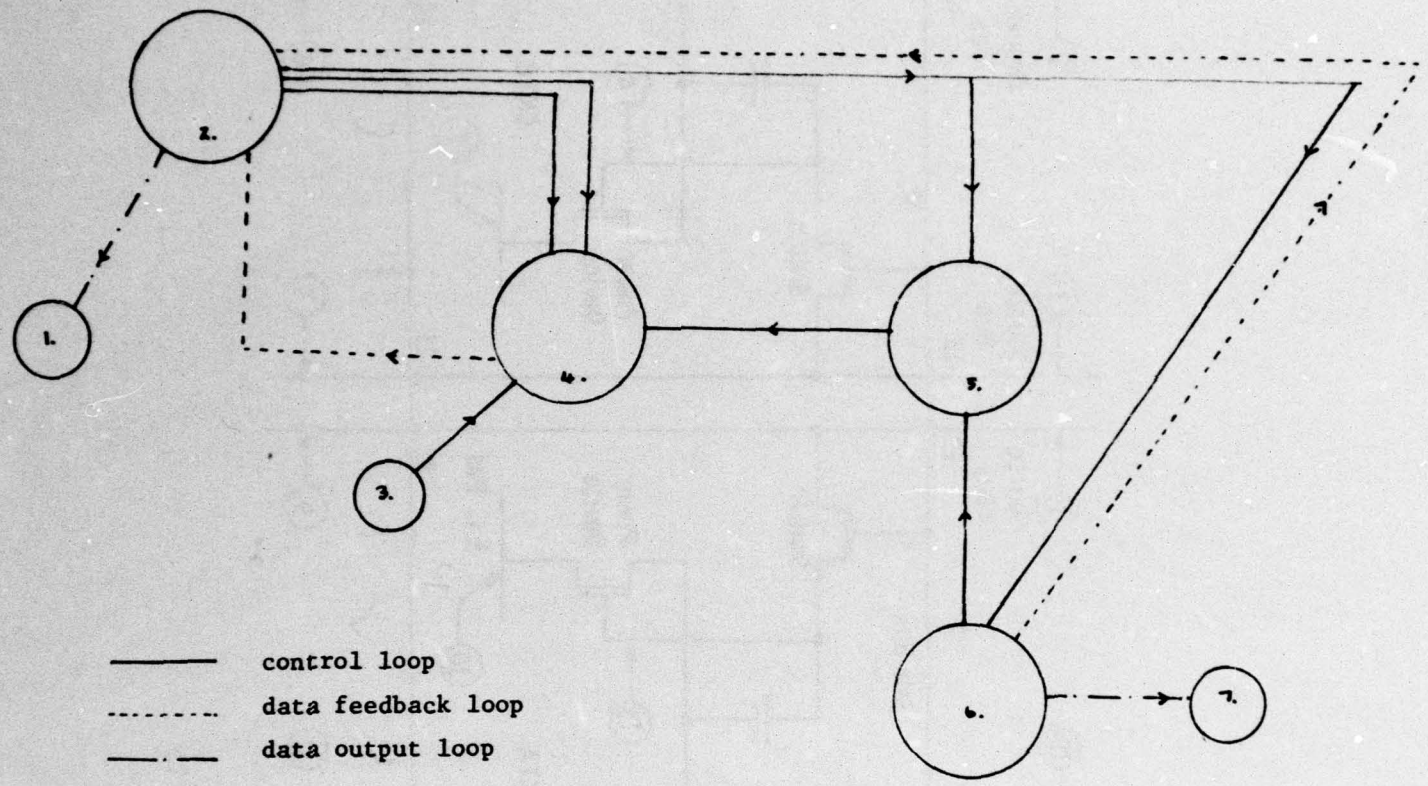
It is also anticipated that the same system could be used to actually repair TF circuits. Fig (14) shows the selected probe positions on a display cell-pair. By selectively grounding the probes in adjacent regions and applying a capacitor generated voltage across a short it is possible to clear it.

3.6. Task IV. Design, Procure and Debug Equipment for Packaging Process

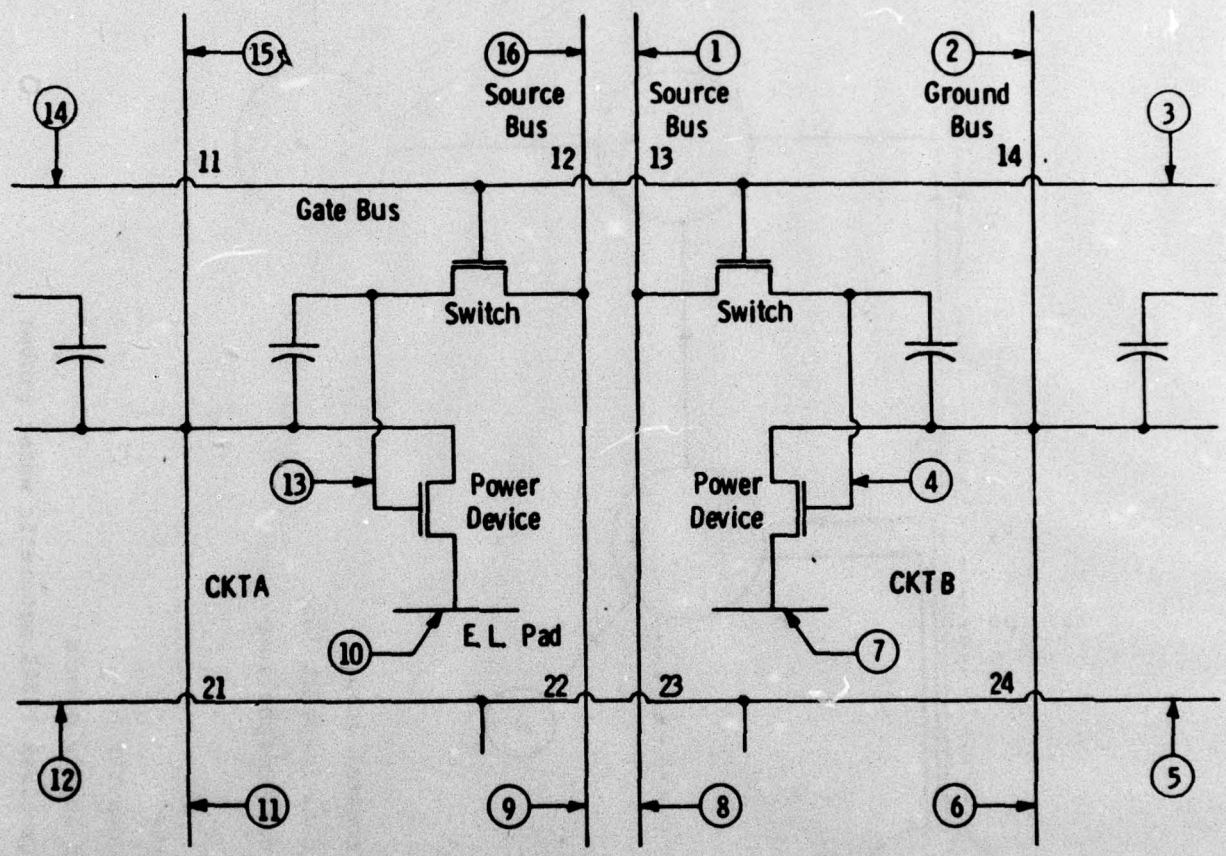
Unlike the circuit fabrication process the subsequent processing is not equipment intensive. Most of the items needed for this process are already in use in this and related programs. The following list details those items that are in a fully debugged and operational state.

(a) Photoresist laminator - existing equipment in operation

(b) Alignment of modules and backing plate seal fixture. This was built for the program and is now in operation.



1. Printer
2. Minicomputer
3. Power supply module
4. Electroglass 1024X automatic wafer prober
5. Relay matrix
6. Test rack,includes four dc supplies and 8kHz ac power
7. Scope output



14. PROBE POSITIONS ON DISPLAY CELL PAIR

(c) Photoresist exposure unit-existing equipment in operation

(d) Photoresist developer - existing equipment in operation

(e) Phosphor spray booth with pressure feed gun and movable substrate system - now in operation

(f) Top electrode evaporator (PbO:Au) - now in operation

In addition the needed cure ovens etc. are in operation. No limitations are evident here to date, if the quantity of displays passing final test increases significantly we may need to build the optional multidisplay frame. As yet this is not needed.

3.7. Task V. Recipe Development for TF Circuit Fabrication Processes

The first attempt at a "production run" of display circuits was begun on October 20, 1976. It was anticipated that the first few runs would be required for debugging new tooling and procedures, and that little or no data relevant to the process would be acquired. Tooling problems did occur: The first substrate fractured near the end of its cycle, leaving pieces of glass on several masks. As a result, several masks were damaged, and none of the four substrates in the run had a complete pattern. The masks have been replaced, and what patterns were available on the substrates were evaluated.

Several problems were anticipated as a result of work carried out by Research Labs personnel. The most serious of these are open interconnect lines due to oxidation of the aluminum overlaps, poor insulator pattern definition due to thermal mask warping, and inclusions in the insulators causing shorts. Resistance measurements of aluminum interconnects yield excellent conductivity, indicating that low level oxygen backfilling during alumina deposition does not cause any measurable oxidation of the interconnect overlaps. Gate and crossover insulator patterns appear quite sharp at the edges of the substrate, but somewhat diffused in the center indicating that tooling or heat may be a serious problem. No conclusions could be reached as to the seriousness of the short problem, due to missing or excessively shadowy

patterns caused by the fractured substrate. Transistor characteristics appear quite reasonable for most of the transistors tested. Switch source-drain leakage measurements were well below 1 na with -20 volt gate bias; power devices were observed to break down at approximately 400 to 450 volts.

The systematic investigation of the short-circuit problem is continuing. Electron microprobe analysis has proved inconclusive so far. An analysis using ion-sputtering yielded only the conclusion that the equipment has poor resolution. The majority of opinion is still that the visible particles are aluminum oxide, because of their location. Discussions have been held with several manufacturers of electron beam guns about evaporating insulators, particularly aluminum oxide. Their consensus seems to be that high voltage EB evaporation of insulators can cause "sputtering," and the obvious solution is to reduce the voltage. The solution had been suggested in the past, along with many others, and had been resisted because of the implications of dual voltage deposition in a single power supply, automated system. However, during the second production run of display circuits on October 27 and 28, electron beam gun accelerating voltage was manually adjusted downward for insulator evaporation for two of the four substrates. Interestingly, the required evaporation rate (5 Å/sec) was achieved with no discernable increase in current (0.12 amps in both cases) even though the accelerating voltage had been reduced from 10 KV to 7 KV! Furthermore, visual inspection of the substrates run at the lower voltage indicates very few or no inclusions in the insulator layers. As a result, a minor modification is being made to the insulator electron beam gun to permit a more reasonable beam pattern at reduced voltage. If further experimental results indicate that low voltage alumina evaporation yields low short-count films, a minor modification to the power control can be made to provide dual voltage capability. The mystery remains however, that a 30% reduction in power achieves the same work (5 Å.sec) as full power. That additional power had to be converted to heat, most of which radiates up to the mask, causing buckling. Thus, if satisfactory control can be achieved

at a lower voltage, and if the resulting films are clean, the lower voltage should also reduce the mask sagging problem.

3.8 Task VI. Recipe Development and Cost Reduction for the Packaging Process

The packaging process consists of photoresist lamination exposure and developing, phosphor and filming resin spray and final top plate seal. No major developments are anticipated here since the process is moderately well defined. Initial experience has confirmed that assumption; our early estimates (Nov. 1975) of yield in this process step indicated that 40% would be reasonable. We now feel that was conservative and we are achieving better than 60% routinely. The major area of difficulty has been the top gold contact to the edge connector, where this evaporated film overlaps the RISTON(R) edge it can become discontinuous. This problem was investigated and it was determined that the sharpness of the edge of the resist was to critical; this in turn was traced to the contrast in the photoplate used to generate the pattern. A photographic emulsion toner was used to soften the contrast at the photoplate edge. We expect this will solve the problem and should know shortly.

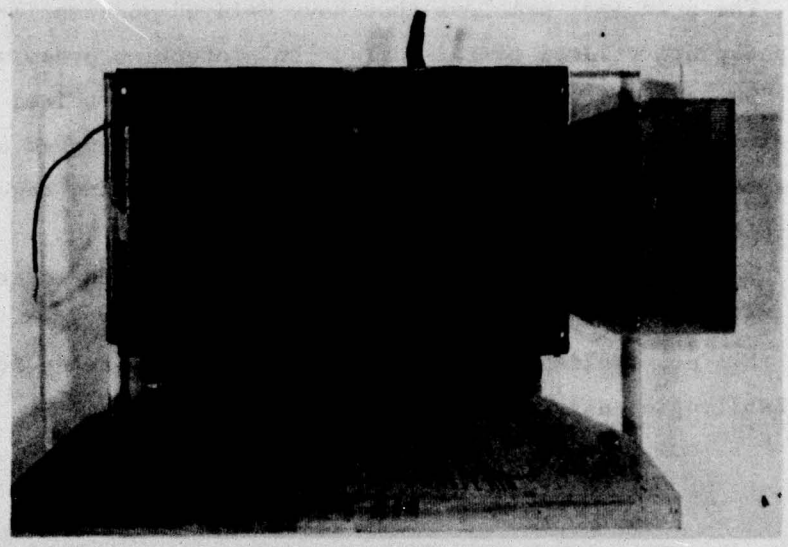
In addition to problem solving we have analyzed the packaging process for it's overall timing. The obvious process step that is the major time consuming stage is the spray of the phosphor. To avoid uneven drying and poor uniformity, and also to maintain the layer thickness limits needed for good control over power dissipation it was found essential to go through several spray/dry stages. The layer being built up from as many as six separate spraying and drying steps. To avoid this time consuming process, which will prevent eventual fullfilment of the production rate objectives, we have started to examine other processes. This is a difficult objective despite its apparent lack of complexity, since in addition to improving the timing and control it is also our objective to enhance the performance of the device. This can be achieved through added contrast between the lit phosphor and the surrounding

areas and therefore is intimately associated with the phosphor and packaging process. A small sub-program to achieve these multiple objectives, consistent with the aims of Task VI (Recipe Development) is now being formalized.

3.9 Task VII. Design, Procure and Debug Equipment for Final Test

Much of the equipment needed for final test already exists. The photometric and environmental equipment being moderately standard. The alphanumeric test exerciser exists in operational form but needed modification to increase the number of lines in the horizontal (from 180 to 222) to mate with the 256 character display. This has been achieved. A simple connection scheme was needed. This was also developed, the device allows repeated insertion and removal without destruction of the contact. It also is reliable. The device is shown attached to a display in Fig (15), is based on an elastomeric multiple redundancy gold contact. The contact interface is made by the AMP Company. It is called "elastomate".

The electronic wattmeter system was linked to the displays fabricated on the program. It worked well and the measurements of power detailed above were made with it.



15. DISPLAY WITH ELASTOMERIC CONTACT JIG

4. CONCLUSIONS

1. The use of an oxidation protection film of noble metal over the aluminum bus bar is required in the laboratory six-station unit but does not, at this point, seem critical in the pilot unit.

2. The principal problems that have delayed success in the laboratory ES phase are related to this oxidation protection process.

3. Successful fabrication of displays, in the required format and using a similar cell layout and material system was achieved using an alternate method. Displays tested to date look promising regarding the requirements of SCS 501.

4. The computer controlled pilot machine has been successfully operated using the new magnetic pull-up fixturing.

5. All new tooling, masks and fixturing is now ready for full display fabrication using the pilot line operation.

5. PROGRAM FOR NEXT QUARTER

1. Install the new tooling and masks on the pilot machine and fabricate first displays under complete computer control.

2. Continue to fabricate ES displays in the laboratory unit with new oxidation protection material system.

3. Obtain modified #7 mask for laboratory ES process, test to establish if this will solve the oxidation/shorting problem.

4. Establish modified phosphor deposition process with the aim of better throughput and improved contrast enhancement.

5. Continue to fabricate displays with X·Y mask method and characterize them regarding the specification requirements of SCS 501.

6. Continue to refine in-process and final test methods.

6. PUBLICATIONS AND REPORTS

None

7. IDENTIFICATION OF PERSONNEL

Overall supervision - M. Green and D. H. Davies

Pilot operation - T. Csakvary, W. L. Rogers, R. E. Stapleton, R. G. Abraham, S. D. Burkholder and J. Gessner

Laboratory ES fabrication - H. Y. Wey, F. S. Youngk, H. B. Shaffer

Laboratory ES fabrication (X-Y) - F. C. Luo and D. W. Yanda

Packaging and performance test - Z.P. Szepesi and D. Leksell

New mask design and fabrication - L. J. Sienkiewicz and M. W. Cresswell

Circuit test - P. R. Malmberg and others listed above

Consultation - T. P. Brody and F. T. Thompson

During the three months reported here the following personnel worked for the following time.

	Approximated Hours Estimated
M. Green	36
D. H. Davies	180
W. L. Rogers	360
R. E. Stapleton	54
R. G. Abraham	18
S. D. Burkholder	325
J. Gessner	360
H. Y. Wey	360
F. S. Youngk	360
Z. P. Szepesi	145
T. Csakvary	300
D. Leksell	180
L. J. Sienkiewicz	36
M. W. Cresswell	7
P. R. Malmberg	110
T. P. Brody	18
F. T. Thompson	3

Note F. C. Luo and D. W. Yanda (X-Y fabrication of displays) are not directly part of the MM&E program. Several of these people were of course charged to the related Westinghouse program other than the MM&TE contract.

DISTRIBUTION LIST

	# of cys
Defense Documentation Center ATTN: DDC-TCA Cameron Station (Bldg 5) Alexandra, VA 22314	2
Commander Naval Electronics Laboratory Cntr ATTN: Library San Diego, CA 92152	1
Commandant, Marine Corps HQ US Marine Corps ATTN: Code AO4C Washington, DC 20380	1
Air Force Avionics Laboratory ATTN: AFAL/DOT, STINFO Wright Patterson AFB, Ohio 45433	1
Chief, USAECOM Field Engr Ofc US Army Electronic Proving Ground ATTN: STEEP-LN-F (Mr. H.A. Ide) Fort Huachuca, AZ 85613	1
US Army Research Office-Durham ATTN: DRDARD-IP Box CM, Duke Station Durham, NC 27706	1
Director Night Vision Laboratory (USAECOM) ATTN: DRSEL-NV-OR (Mr. S. Segal) Fort Belvoir, VA 22060	1
Commanding General US Army Electronics Command Fort Monmouth, NJ 07703	
DRSEL-TL-BD	3
DRSEL-TL-B	1
DRSEL-PP-I-PI-1 (E. Mason)	2
Sylvania Electronic Systems Western Division ATTN: Technical Reports Library PO Box 205 Mountain View, CA 94040	1
Advisory Group on Electron Dev. 201 Varick St., 9th Floor New York, NY 10014	2
Metals and Ceramics Information Cntr Battelle Memorial Institution 505 King Avenue Columbus, Ohio 43201	1
Electronic Properties Info Cntr Hughes Aircraft Company Centinela and Teale Streets Culver City, CA 90230	1
Dr. Egon Loebner Hewlett-Packard Co. 1501 Page Mill Road Palo Alto, CA 94304	1
PMO ARTADS DRCPM-TOS-SE ATTN: MAJ Oswandel Fort Monmouth, NJ 07703	1
Dr. Benjamin Kazan Xerox Research Labs 3333 Coyate Hill Dr Palo Alto, CA 94304	1
Dr. James H. Becker Xerox Corporation Xerox Square W-130 Rochester, NY 14603	1
Dr. J. E. Bigelow General Electric Co. Corporate Research and Dev Cntr Bldg 37, Room 255 Schnectady, NY 12301	1
Dr. L. Tannas Rockwell International 3370 Miraloma Avenue Anaheim, CA 92803	1

DISTRIBUTION LIST

	# of cys
Charles Blank ISCP Rome Air Development Cntr Griffiss AFB, NY 13441	1
Dr. J. Hanak RCA Research Center Princeton, NJ 08540	1
Mr. G. Fugate Aerojet Electrosystems Co. 1100 W. Hollyvale Street Azusa, CA 91702	1
Dr. L. T. Lipton Hughes Aircraft Company Industrial Products Division 6855 El Camino Real Carlsbad, CA 92008	1
A. Rosengreen SRI - Bldg 404E 333 Ravenswood Avenue Menlo Park, CA 94025	1
Dr. Stewart Kurtz Philips Laboratories 345 Scarborough Road Briarcliff Manor, NY 10510	1
Ofc, Asst Sec of the Army (R&D) ATTN: Asst for Research Room 3E-379, Pentagon Washington, DC 20310	1
Commanding General US Army Materiel Dev & Read Cmd ATTN: DRCRD-H Washington, DC 20315	1
Commanding General US Army Missile Command ATTN: DRSMI-RR (Dr. J.P. Hallowes) Redstone Arsenal, AL 35809	1
Mr. J. C. Erskine, Res. Dept Zenith Radio Corp 6001 W. Dickens Avenue Chicago, IL 60639	1